IN THE CLAIMS

1-20. (Canceled)

21. (New) A method for transferring data in an information processing system having a processor bus, a processor coupled to said processor bus, a memory bus, a memory unit coupled to said memory bus, a system bus, a device coupled to said system bus, a data transfer unit coupled to said processor bus and said memory bus and said system bus, said method comprising the steps of:

outputting, by said processor, a data transfer request including an address to said processor bus;

receiving said data transfer request by said data transfer unit that enables a transfer of data between any arbitrary two of said processor, said main memory and said display control device via a corresponding two of said processor bus, said memory bus and said I/O bus;

outputting a signal in order to access the memory unit by said data transfer unit according to said data transfer request output from said processor to said memory bus if said address corresponds to an address assigned to said memory unit,

outputting a signal in order to access the device by said data transfer unit according to said data transfer request

output from said processor to said system bus if said address corresponds to an address assigned to said device;

receiving said data output from said memory unit or said device; and

outputting said data to said processor by said data transfer unit.

22. A method for transferring data in an information processing system according to claim 21, wherein at least one of said processor bus, said memory bus and said system bus is an address/data multiplexed bus.

23. A method for transferring data in an information processing system according to claim 21, wherein said device is a disk file controller.

24. A method for transferring data in an information processing system according to claim 21, wherein said device is a controller for drawing and displaying images.

25. A method for transferring data in an information processing system according to claim 21, wherein said device is a controller for networks and communication.

26. A method for transferring data in an information processing system according to claim 21, wherein

each of said processor bus, said memory bus, and said system bus has a data bus for transferring said data, an address bus for transferring said address, and a control bus for transferring control signals, and

said data transfer unit includes:

a transfer circuit coupled to said data buses of said processor bus, said memory bus, and said system bus for transferring said data through said data buses, and

a control circuit coupled to said address bus of said processor bus for controlling said transfer circuit in accordance with said address provided from said processor via said address bus of said processor bus.

27. A method for transferring data in an information processing system having a processor bus, a processor operatively coupled to said processor bus, a memory bus, a memory unit operatively coupled to said memory bus, a system bus, a device operatively coupled to said system bus, a data transfer unit coupled to said processor bus and said memory bus and said system bus, said method of comprising the steps of:

outputting, by said processor, a data transfer request including an address to said processor bus;

receiving said data transfer request by said data transfer unit that enables a transfer of data between any arbitrary two of said processor, said main memory and said display control device via a corresponding two of said processor bus, said memory bus and said I/O bus;

outputting a signal in order to access the memory unit by said data transfer unit according to said data transfer request output from said processor to said memory bus if said address corresponds to an address assigned to said memory unit;

outputting a signal in order to access the device by said data transfer unit according to said data transfer request output from said processor to said system bus if said address corresponds to an address assigned to said device;

receiving said data output from said memory unit or said device; and

outputting said data to said processor by said data transfer unit.

28. A method for transferring data in an information processing system according to claim 27, wherein at least one

of said processor bus, said memory bus and said system bus is an address/data multiplexed bus.

29. A method for transferring data in an information processing system according to claim 27, wherein said device is a disk file controller.

30. A method for transferring data in an information processing system according to claim 27, wherein said device is a controller for drawing and displaying images.

31. A method for transferring data in an information processing system according to claim 27, wherein said device is a controller for networks and communication.

32. A method for transferring data in an information processing system according to claim 27, wherein

each of said processor bus, said memory bus, and said system bus has a data bus for transferring said data, an address bus for transferring said address, and a control bus for transferring control signals, and said data transfer unit includes:

a transfer circuit coupled to said data buses of said processor bus, said memory bus, and said system bus for transferring said data through said data buses; and

a control circuit coupled to said address bus of said processor bus for controlling said transfer circuit in accordance with said address provided from said processor via said address bus of said processor bus.

33. A method for transferring data in an information processing system having a processor bus, a processor operatively coupled to said processor bus, a memory bus, a memory unit operatively coupled to said memory bus, a system bus, a device operatively coupled to said system bus, a data transfer unit coupled to said processor bus and said memory bus and said system bus, said method comprising the steps of:

outputting, by said processor, a data transfer request including an address to said processor bus;

receiving said data transfer request by said data transfer unit that enables to execute one of data transfer modes which includes a first mode in which data is transferred between said processor and said memory unit, a second mode in which data is transferred between said device and said memory unit, a third mode in which data is transferred between said processor and said device;

outputting a signal in order to access the memory unit by said data transfer unit according to said data transfer request output from said processor to said memory bus if said address corresponds to an address assigned to said memory unit in said first mode;

outputting a signal in order to access the device by said data transfer unit according to said data transfer request output from said processor to said system bus if said address corresponds to an address assigned to said device in said third mode;

receiving said data output from said memory unit or said device in said first mode or third mode; and

outputting said data to said processor by said data transfer unit.

34. A method for transferring data in an information processing system according to claim 33, wherein at least one of said processor bus, said memory bus and said system bus is an address/data multiplexed bus.

35. A method for transferring data in an information processing system according to claim 33, wherein said device is a disk file controller.

36. A method for transferring data in an information processing system according to claim 33, wherein said device is a controller for drawing and displaying images.

37. A method for transferring data in an information processing system according to claim 33, wherein said device is a controller for networks and communication.

38. A method for transferring data in an information processing system according to claim 33, wherein

each of said processor bus, said memory bus, and said system bus has a data bus for transferring said data, an address bus for transferring said address, and a control bus for transferring control signals, and said data transfer unit includes:

a transfer circuit coupled to said data buses of said processor bus, said memory bus, and said system bus for transferring said data through said data buses, and

a control circuit coupled to said address bus of said processor bus for controlling said transfer circuit in accordance with said address provided from said processor via said address bus of said processor bus.